IN THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 17 as follows:

Electrostatic discharge~~,~~ ("ESD" hereafter)~~,~~ is a common phenomenon that occurs during handling of semiconductor IC devices. An electrostatic charge may accumulate for various reasons and cause potentially destructive effects on an IC device. Damage typically can occur during a testing phase of its fabrication, during assembly of the IC onto a circuit board, ~~as well as~~ and during use of equipment into which the IC has been installed. Damage to a single IC due to poor ESD protection in an electronic device can hamper some of its designed functions, or sometimes all of them. ESD protection for semiconductor ICs is, therefore, a reliability problem. In order to prevent this, various electrostatic breakdown protection techniques have been proposed. As one such technique discloses, Japanese Patent Application Kokai Publication No. Hei 7-086510 is a semiconductor device that is equipped with a common discharge line (CDL).

Please amend the paragraph beginning at page 2, line 23 as follows:

FIG. 1A shows a conventional gate-grounded NMOS field-effect transistor that is commonly used in ESD protection circuit design, wherein its gate electrode is tied to its source electrode at node 10 and connected to the ground, GND. The current-voltage, I-V, characteristics of the gate-grounded NMOS field-effect transistor is shown in FIG. 1B. ~~referring~~ Referring to what is shown in FIG. 1B, the voltage V across the drain and source electrode of the gate-grounded NMOS field-effect transistor, shown in FIG. 1A, is greater than the threshold voltage V_{t1}, referring to point A, the gate-grounded NMOS field-effect transistor is then triggered. The gate-grounded NMOS field-effect transistor

snapback at point B where the voltage V reaches V_{sb} value, moreover, it enters the second breakdown region at point C where the voltage V is at V_{t2} value. Once the gate-grounded NMOS field-effect transistor enters the second breakdown region, thermal runaway will occur, ~~hence~~ easily ~~result~~ resulting in device damages.

Please amend the paragraph beginning at page 4, line 3 as follows:

Conversely, when an ESD stress having a negative polarity with respect to Pad 1 arises at Pad 2, the associated ESD voltage is coupled to a gate-grounded NMOS field-effect transistor N_1, and thus triggers the NMOS field-effect transistor N_1 to be operated in snapback mode. Consequently, a great amount of ESD discharge current I_2 flows from Pad 1, through the common discharge line 30 and then to Pad 2, because the diode D_2 is forward biased. This symmetrical characteristic of the discharge path ~~in~~ which accompanies ~~with~~ the simplification in ESD protection design contributes to the advantages of using CDL structure in ESD protection design.

Please amend the paragraph beginning at page 4, line 13 as follows:

Nevertheless, the triggering voltage of using a gate-grounded NMOS field-effect transistor and a diode as ESD elements ~~in~~ between a Pad and the common discharge line is too high to protect submicron IC devices in the conventional method. Moreover, as mentioned earlier, once the gate-grounded NMOS field-effect transistor enters the second breakdown region, thermal runaway is likely to occur, hence easily ~~result~~ results in device damages. Furthermore, ESD protection by using the conventional method is easily restricted in the CMOS process, this is because the channel length of the gate-

grounded NMOS field-effect transistor needs to be smaller than the output NMOS for making sure that the gate-grounded NMOS field-effect transistor ~~breakdown~~ breaks down before the output NMOS.

Please amend the paragraph beginning at page 5, line 7 as follows:

An object of the present invention is to substantially ~~obviate~~ eliminate one or more of the problems caused by limitations and disadvantages of the related art.

Please amend the paragraph beginning at page 5, line 10 as follows:

Another object of the present invention is to provide an ESD protection network having a triggering voltage and a holding voltage lower than that of the conventional design, which can effectively made submicron IC devices immune to ESD damage.

Please amend the paragraph beginning at page 5, line 14 as follows:

A further object of the present invention is to provide an enhanced ESD protection performance apparatus, which is equipped with a common discharge line, for protecting VLSI circuits and particularly CMOS devices.

Please amend the paragraph beginning at page 8, line 17 as follows:

FIG. 2C shows the I-V characteristics of the low triggering voltage SCR with zener diode depicts in both FIG. 2A and 2B. Referring to FIG. 2C, one can see that when the voltage V across the anode and the cathode of the low triggering voltage SCR of both FIG. 2A and 2B is greater than the threshold voltage V_{t3}. Referring to point D,

the SCR is then triggered. Sequentially, a low-holding voltage V_h is quite low, and the resulting power consumption is small. In the mean-while, using a zener diode as a triggering element makes the SCR have a much lower triggering voltage at point D as compared to the conventional element at point A.

Please amend the paragraph beginning at page 9, line 3 as follows:

FIG. 3 schematically depicts a semiconductor device with a modified CDL (Common Discharge Line) ESD (Electrostatic Discharge) protection circuitry of an embodiment of the present invention, which utilizes the low triggering voltage SCR with zener diode as depicted in FIG. 2A. The semiconductor device comprises a plurality of bonding pads 300, 310 and 320, possibly a mixture of input pads, output pads, V.sub.DD pads, and/or V.sub.SS pads, each having at least one connecting terminal 301, 311 and 321; a common discharge line 330 with an open-ended design. ~~That~~ that is, neither grounded nor connected to any source; and a protective device 302, 312 and 322 connected between the connecting terminal of at least one bonding pad and the common discharge line. The protective devices 302, 312 and 322 are connected between the connecting terminal of at least one bonding pad and the common discharge line. The protective devices 302, 312 and 322 each includes a silicon-control-rectifier used for electrostatic discharge protection and a zener diode Z.sub.1, Z.sub.2 and Z.sub.n for lowering a trigger voltage of the silicon-control-rectifier.

Please amend the paragraph beginning at page 11, line 11 as follows:

In conclusion, a semiconductor device having ~~the~~ electrostatic discharge protective circuitry adapted to a common discharge line (CDL) is disclosed by the present invention with two embodiments. ~~Wherein,~~ wherein the intrinsic symmetrical characteristics of the discharge path ~~in accompanies with~~ is accompanied by the simplification in ESD protection design of using CDL structure having been brought into practice fully in ESD protection design by the invention.

Please amend the paragraph beginning at page 11, line 18 as follows:

Of course, it is possible to apply the present invention to the ESD protection network with a SCR, and also it is possible for the present invention to protect any one ESD circuit and effectively ~~making~~ make submicron IC devices immune to ESD damage. Also, this invention can be applied to provide the SCR with the zener diodes concerning ESD protection circuit used for protecting the device has not developed at present. The ESD structure of the present invention is the best integrated circuit structure.